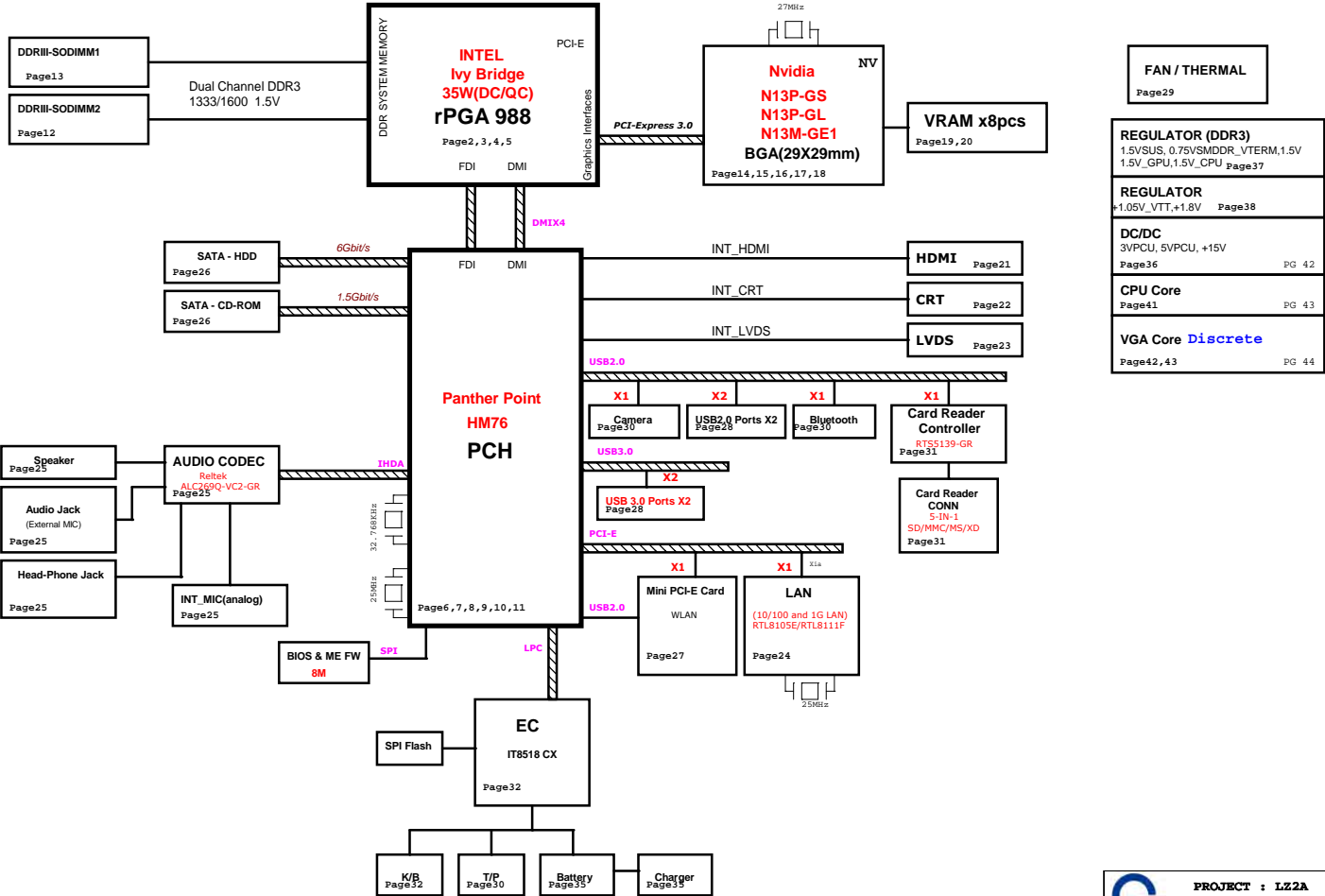
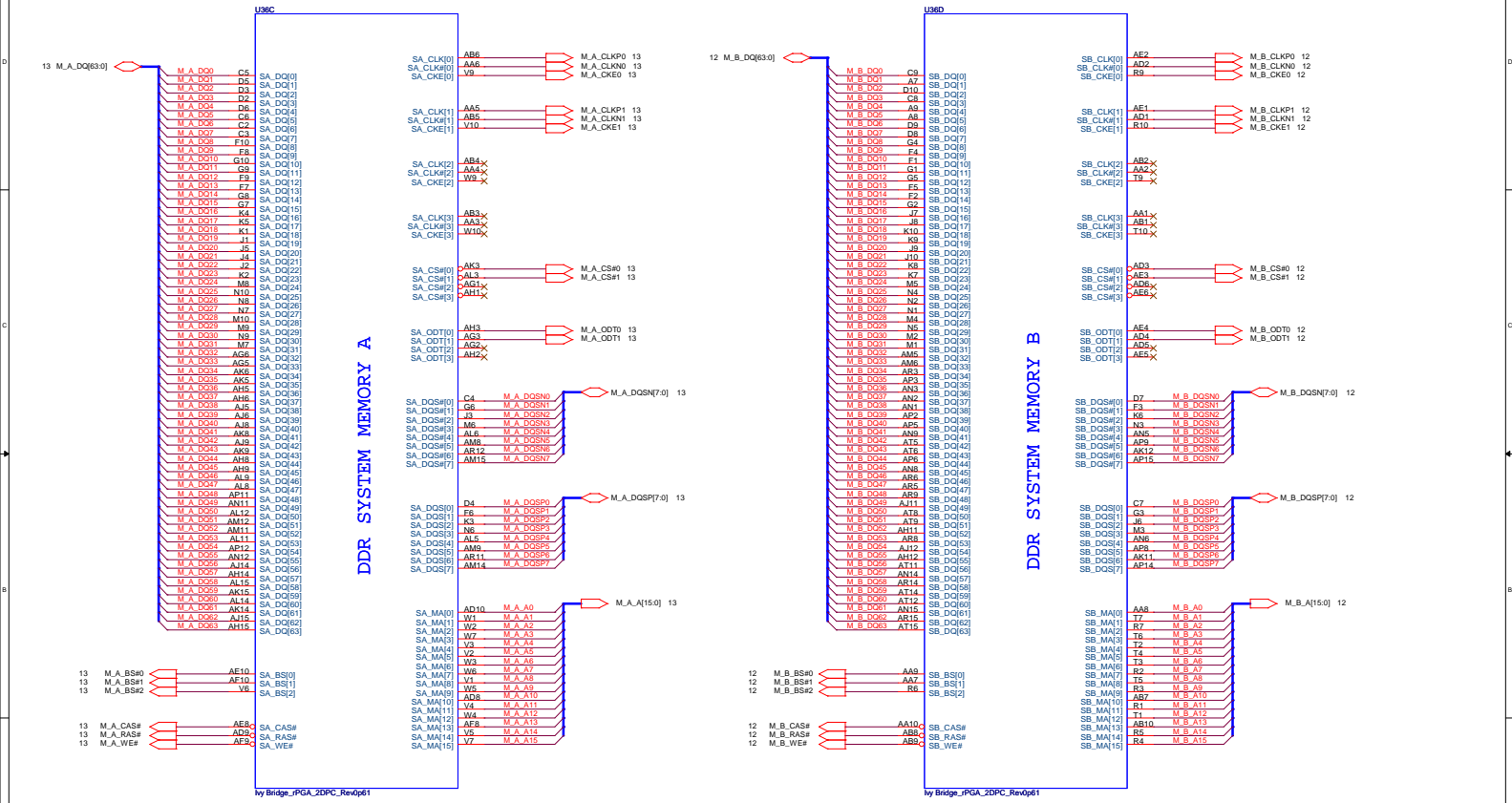
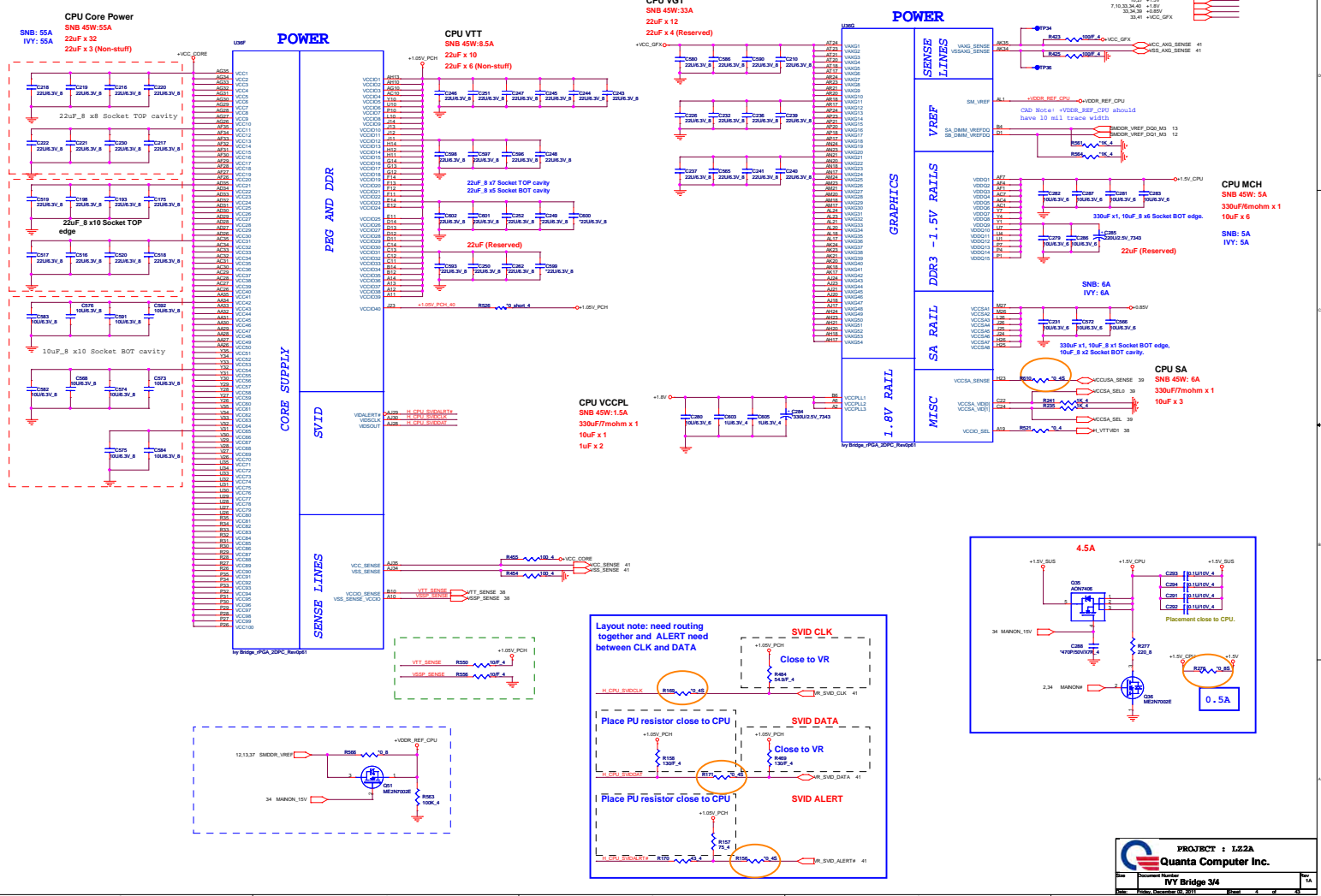
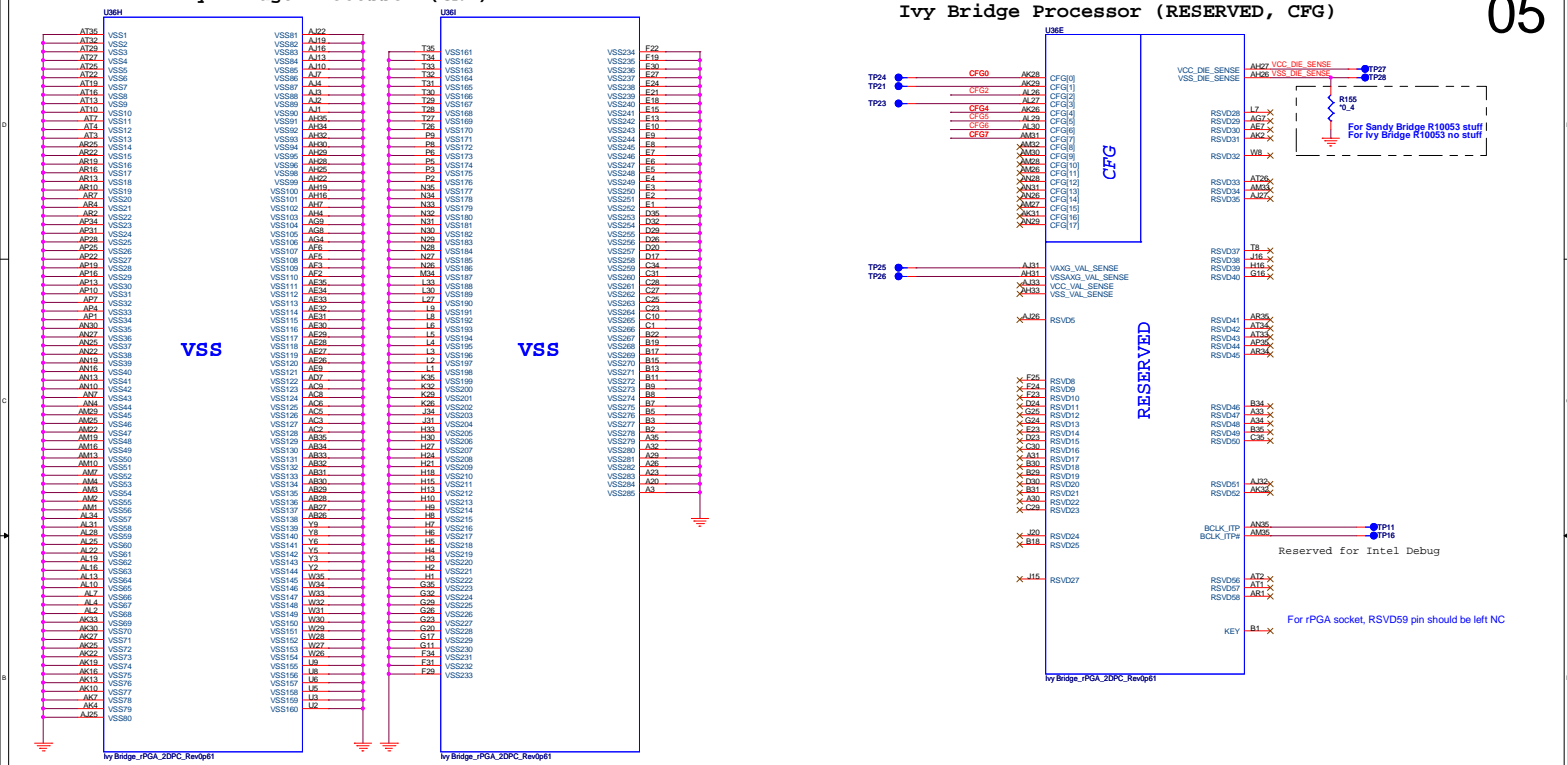


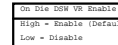
LZ3/LZ3A (Z580) Intel Chief River Platform (Optimus) Block Diagram

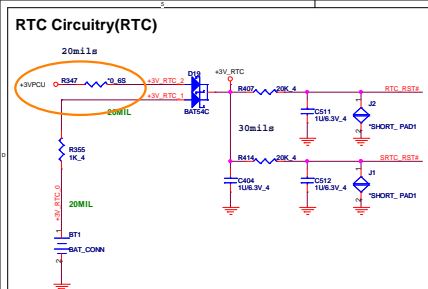




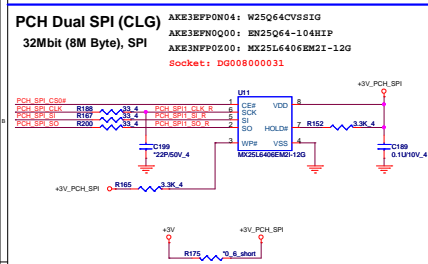
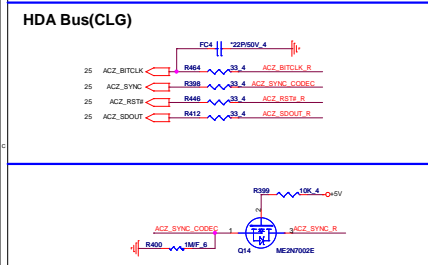
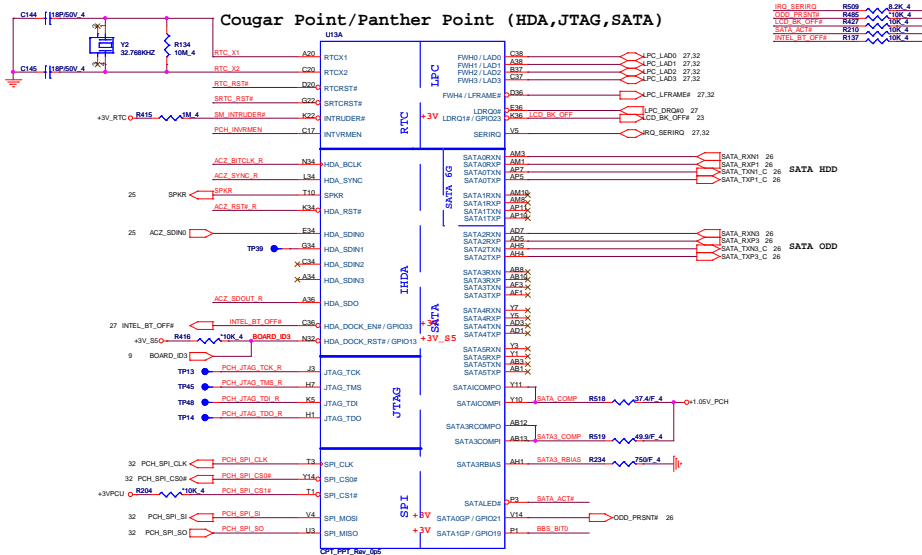








PCH2 (CLG)

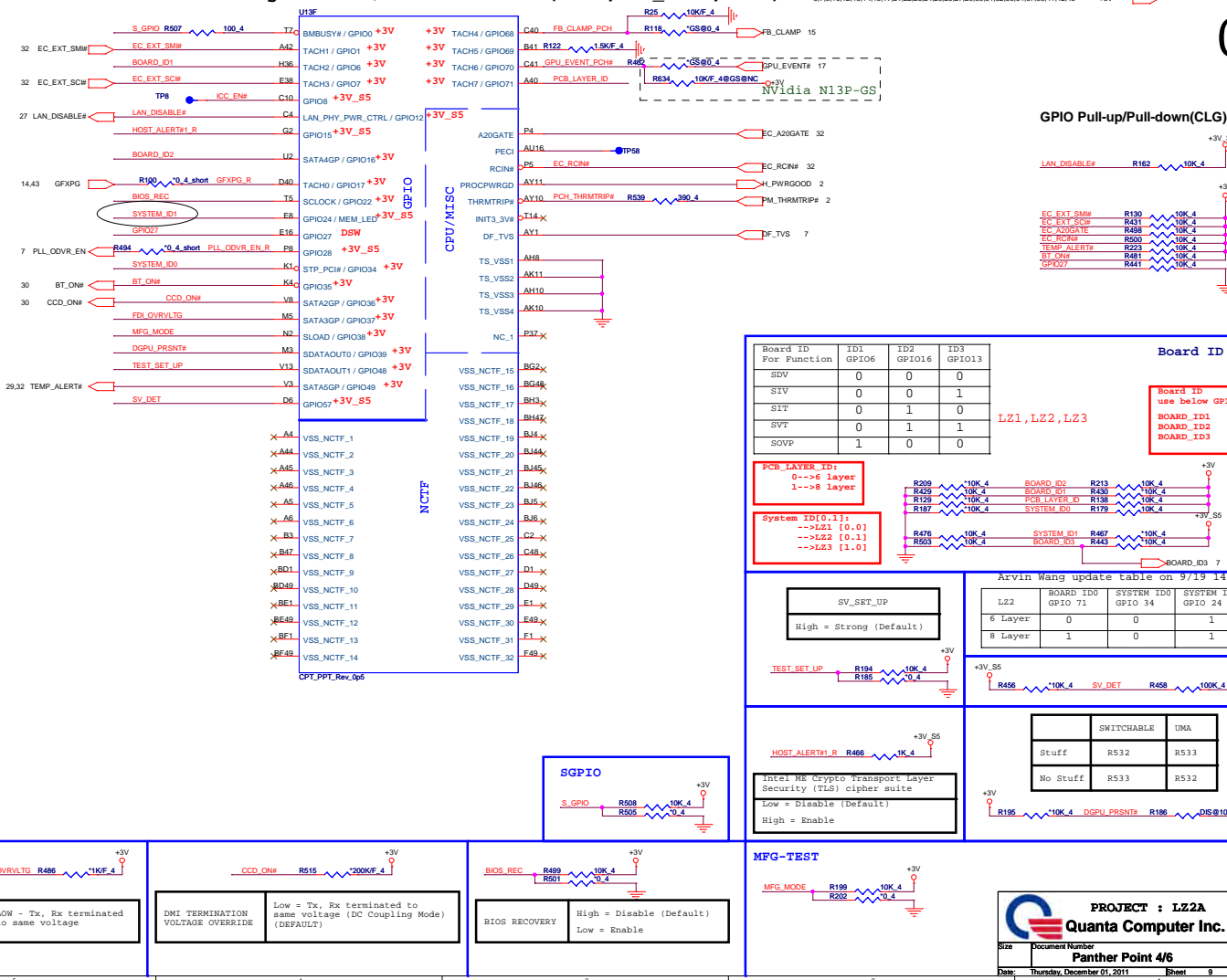


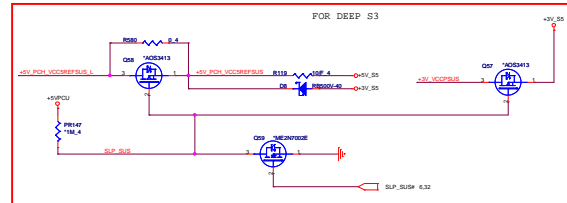
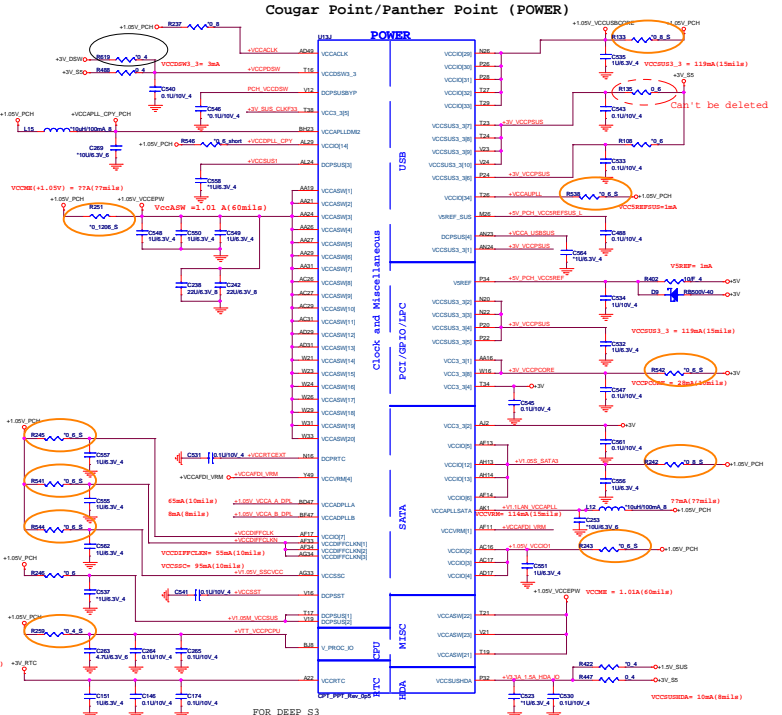
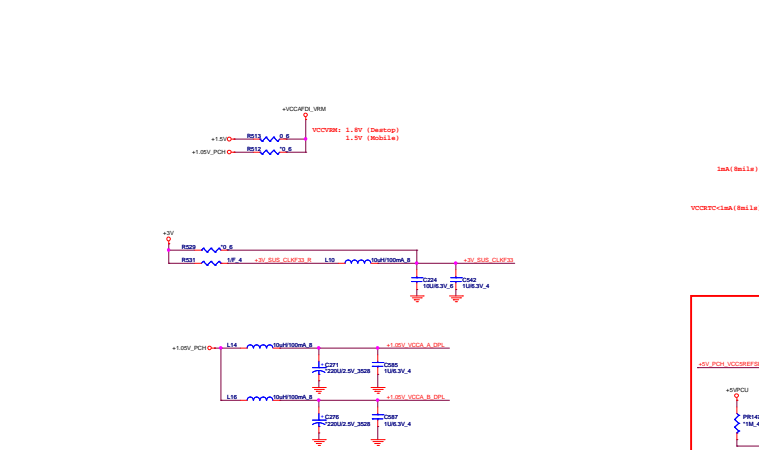
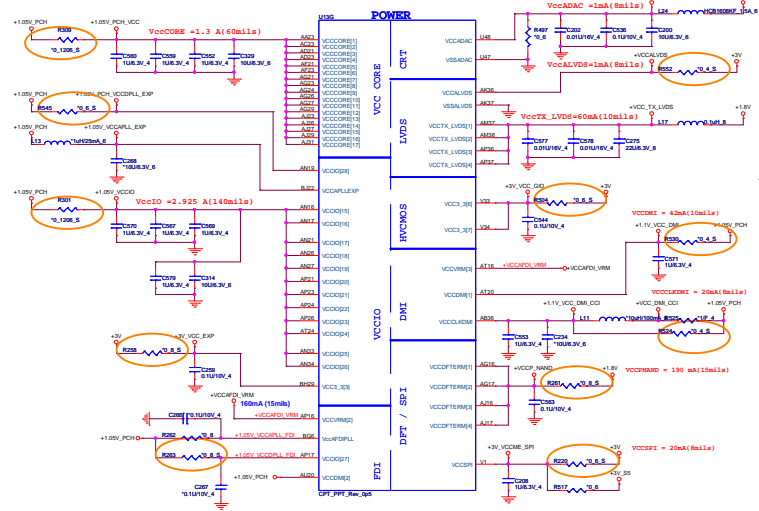
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration										
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V_PCH_RTC R514 10K 4 SPKR									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R472 10K 4 PC1_GNT3# 8									
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R114 300K 4 PCH_INVRMEN									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table><tr><th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr><tr><td>1</td><td>1</td><td>SPI *</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></table>	GNT1#	GNT0#	Boot Location	1	1	SPI *	0	0	LPC	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]
GNT1#	GNT0#	Boot Location											
1	1	SPI *											
0	0	LPC											
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		R471 10K 4 BIOS_BT1 8 R203 10K 4 BIOS_BT0									
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	+3V_SS R411 10K 4 ACZ_SDOOUT_R									
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R254 10K 4 CH1_BV R255 10K 4 DF_TVS 9 CH1_BV 1.8V									
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R400 10K 4 PLL_COVR_EN 9									
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_SS R413 10K 4 ACZ_SYNC_R									
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)										
SPI_MOSI	ITPM function Disable	APWROK	0 = Enable (weak pull-down 20K) 1 = Default	+3V_PCH_RTC R181 10K 4 PCH_SPI_B									
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)										

1/1/2020 <https://www.gutenberg.org/files/54282/54282-h/54282-h.htm>








Cougar Point/Panther Point (GND)

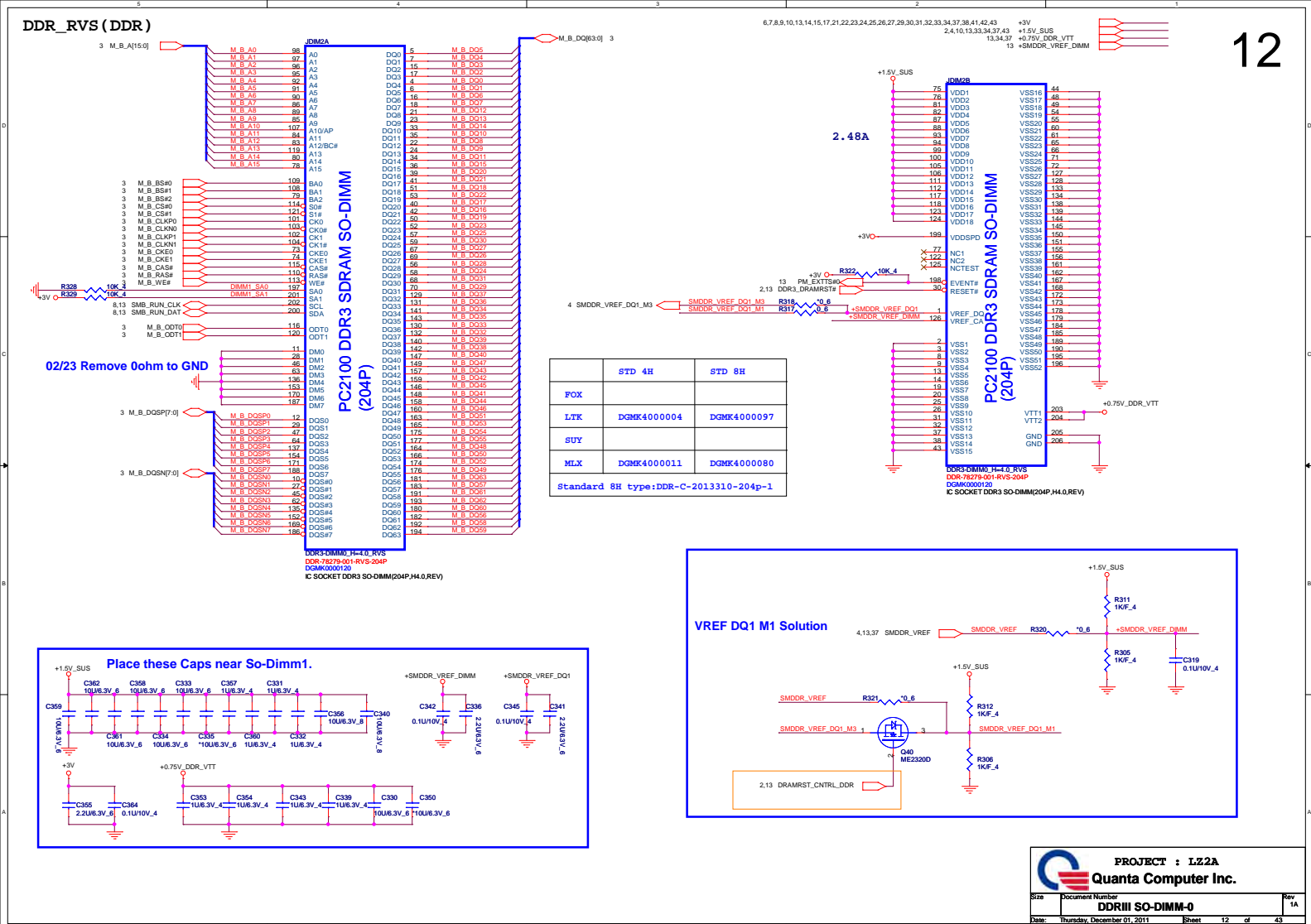
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AA2	VSS11
AA3	VSS12
AA34	VSS13
AA34	VSS14
AA34	VSS15
AA34	VSS16
AA34	VSS17
AA34	VSS18
AA34	VSS19
AA34	VSS20
AA34	VSS21
AA34	VSS22
AA34	VSS23
AA34	VSS24
AA34	VSS25
AA34	VSS26
AA34	VSS27
AA34	VSS28
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AA34	VSS39
AA34	VSS40
AA34	VSS41
AA34	VSS42
AA34	VSS43
AA34	VSS44
AA34	VSS45
AA34	VSS46
AA34	VSS47
AA34	VSS48
AA34	VSS49
AA34	VSS50
AA34	VSS51
AA34	VSS52
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AA34	VSS80

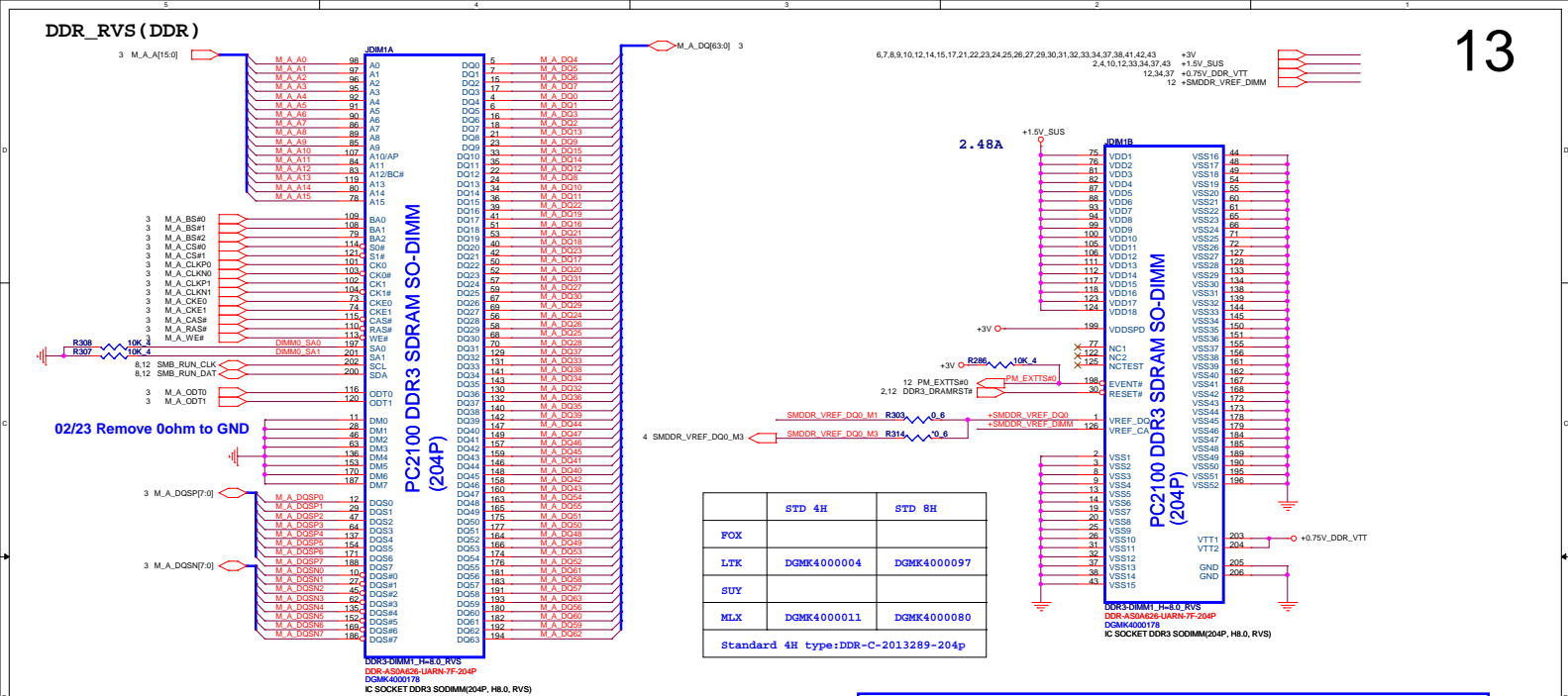
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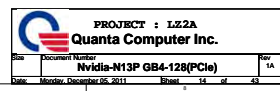
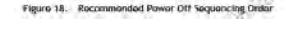
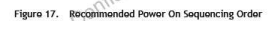
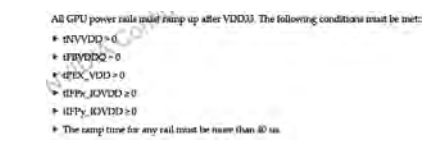
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AA4	VSS161
AA4	VSS162
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AA4	VSS166
AA4	VSS167
AA4	VSS168
AA4	VSS169
AA4	VSS170
AA4	VSS171
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AA4	VSS258

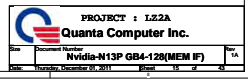
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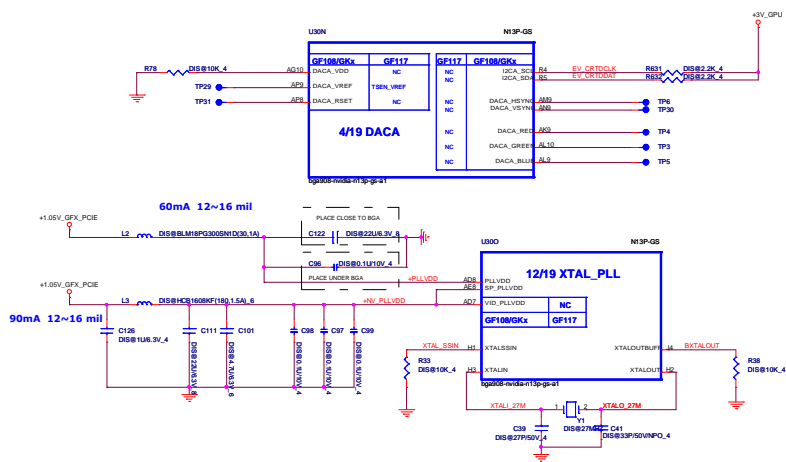
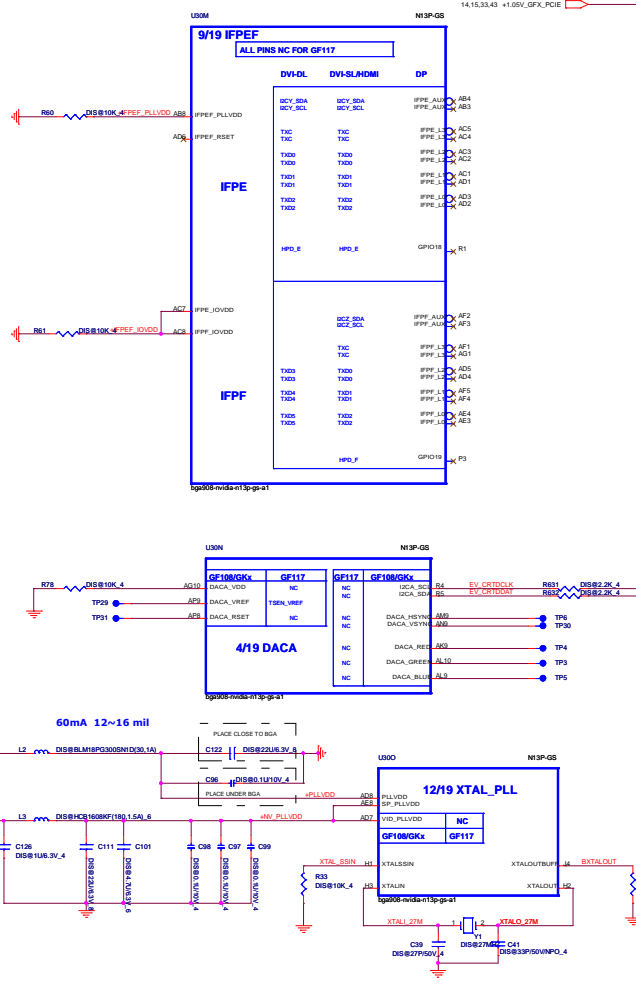
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Quanta Computer Inc.					
Size	Document Number		Rev	1A	
Panther Point 6/6					
Date:	Thursday, December 01, 2011	Sheet	11	of	43

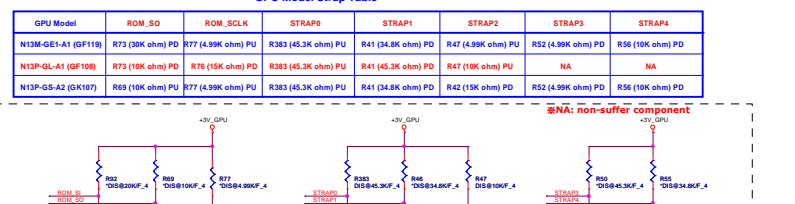
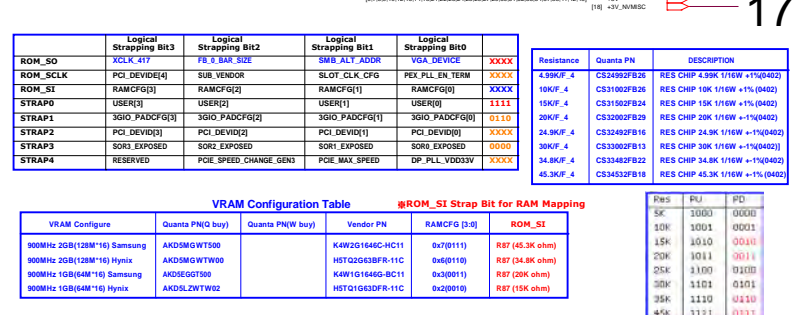




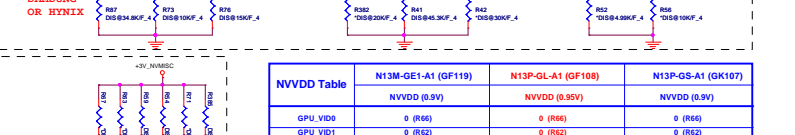


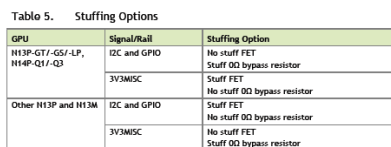
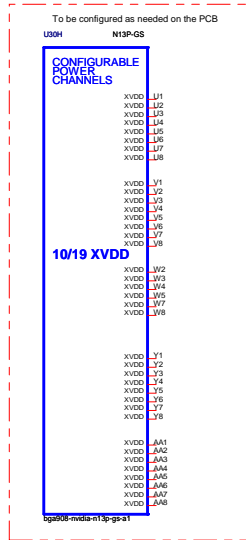







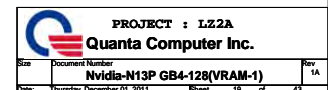
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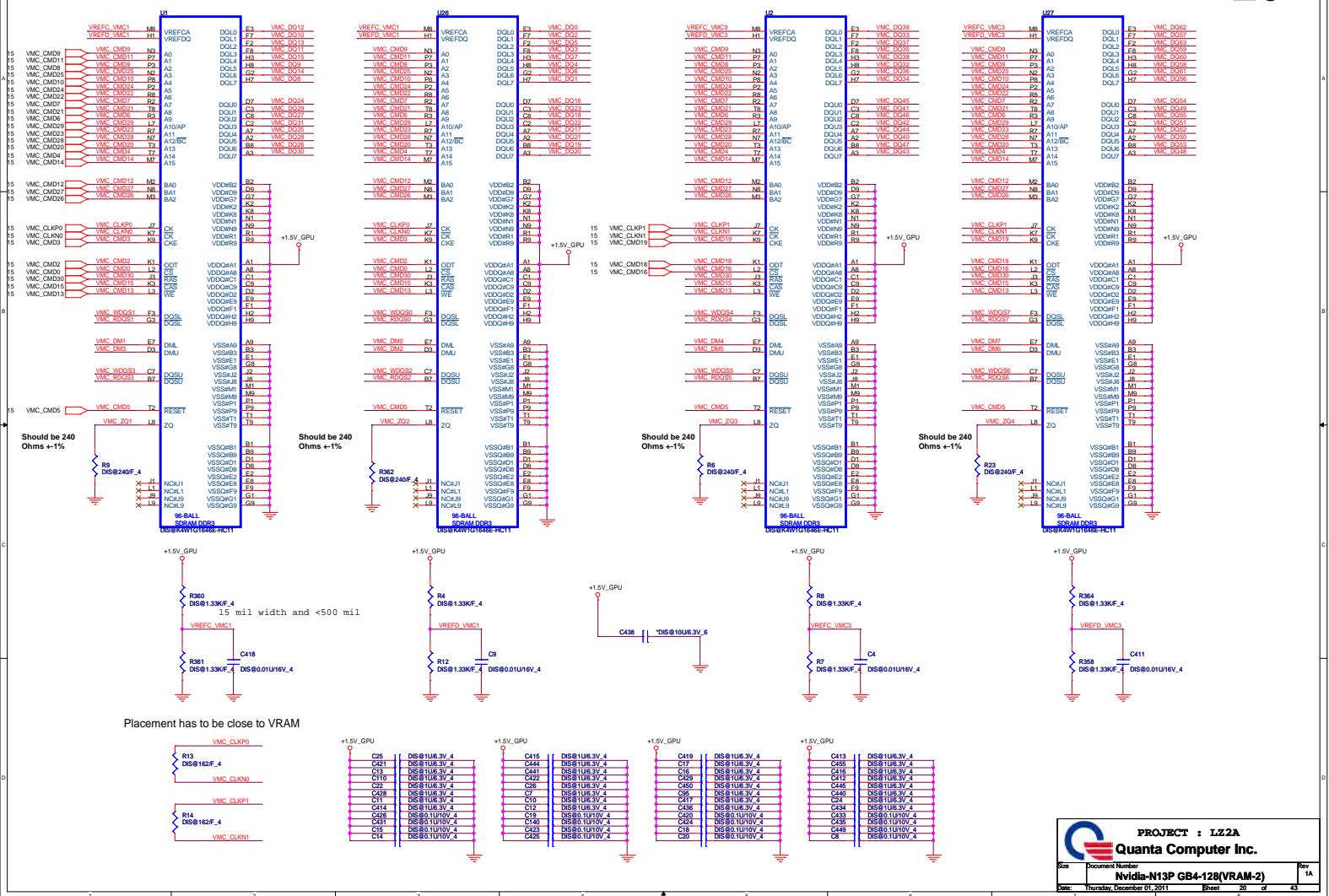
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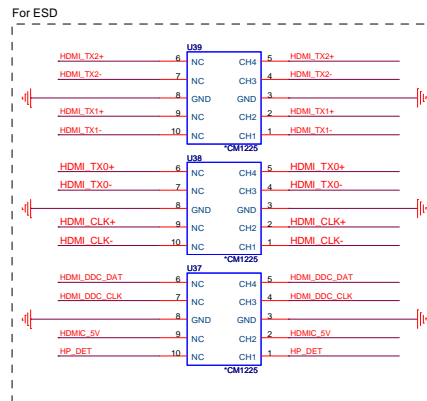
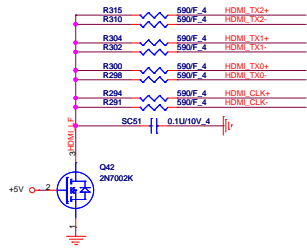
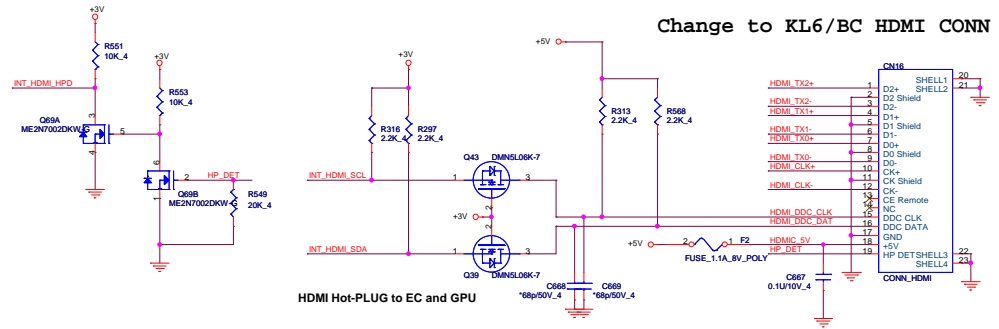
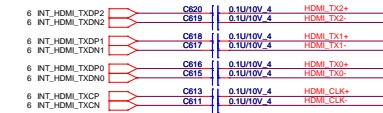


GPU	Signal/Rail	Stuffing Option
H13P-GT/-GS/-LP, H14P-Q1/-Q3	I2C and GPIO	No stuff FET Stuff OQ bypass resistor
	3V3MISC	Stuff FET No stuff OQ bypass resistor
Other H13P and H13M	I2C and GPIO	Stuff FET No stuff OQ bypass resistor
	3V3MISC	Stuff FET No stuff OQ bypass resistor

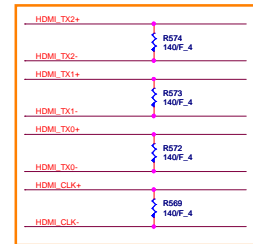
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Size	Document Number		Rev 1A
Nvidia-N13P GB4-128(POWER)			
Date:	Thursday, December 01, 2011	Sheet	18 of 43

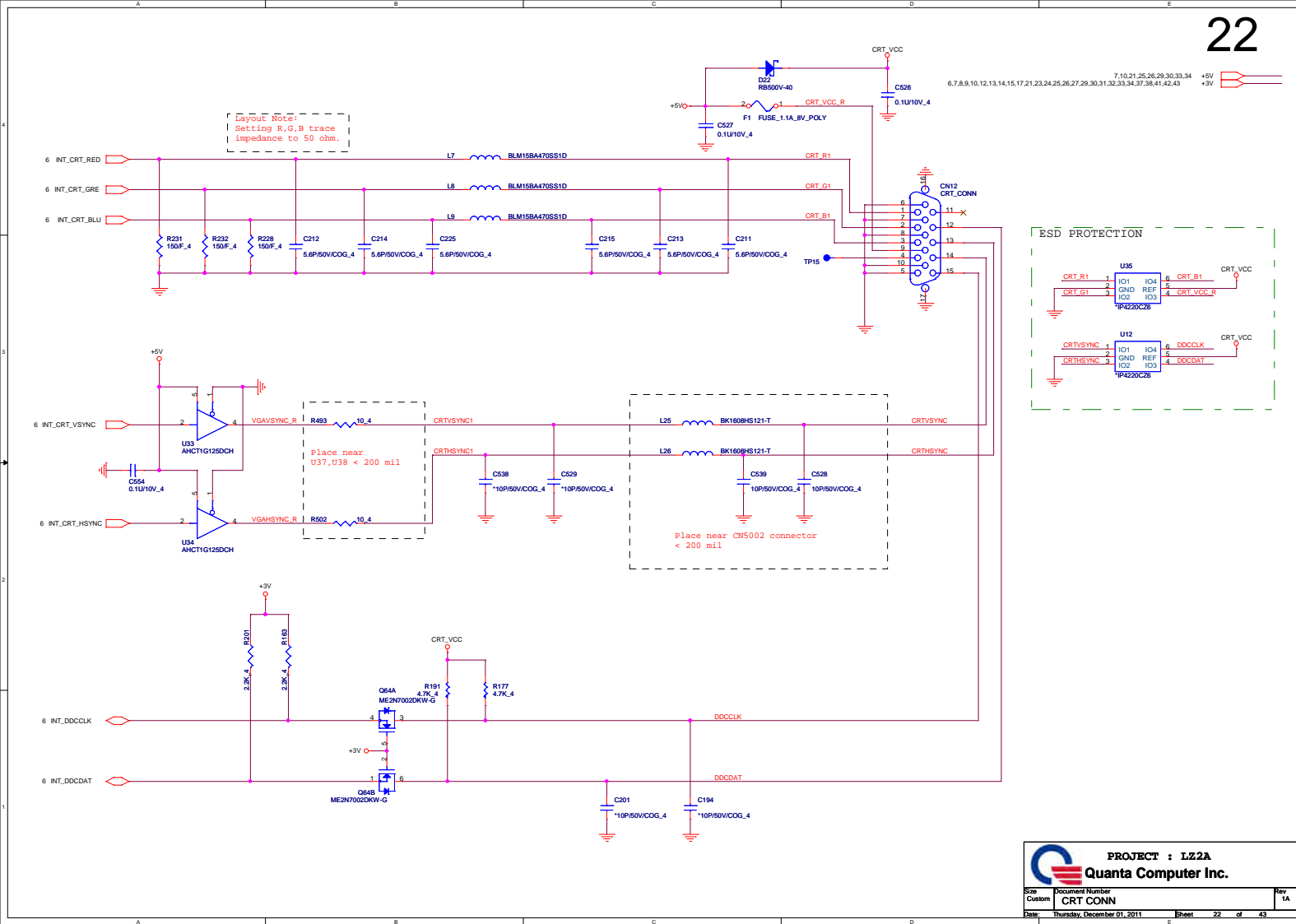




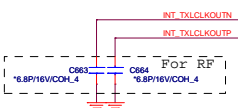
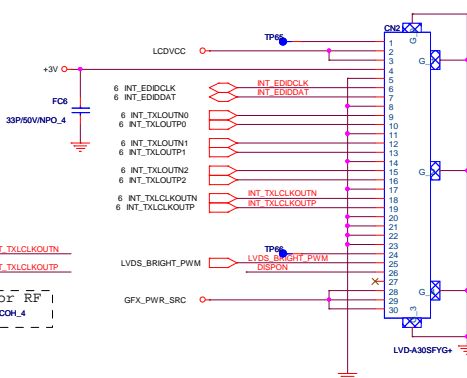
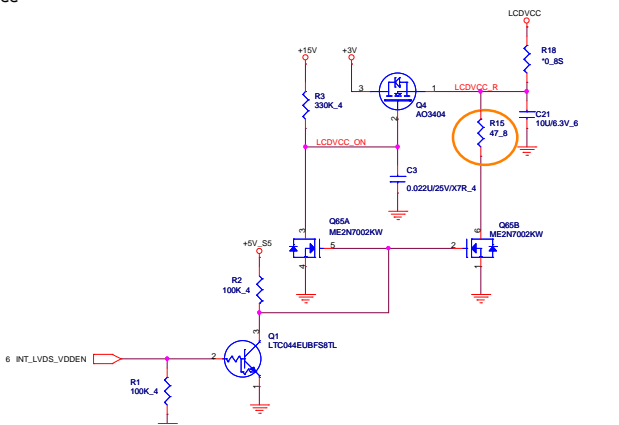


EMI reserve for HDMI

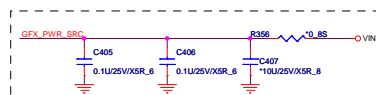
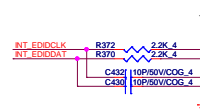
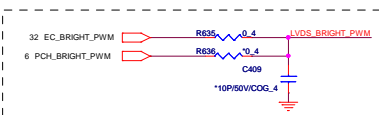
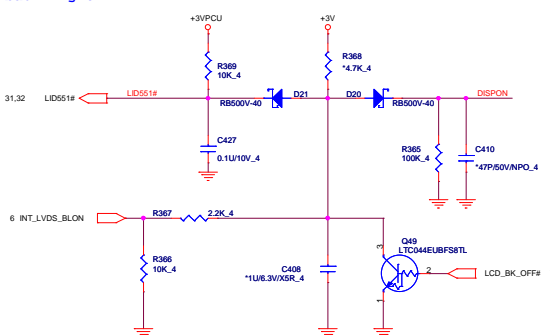





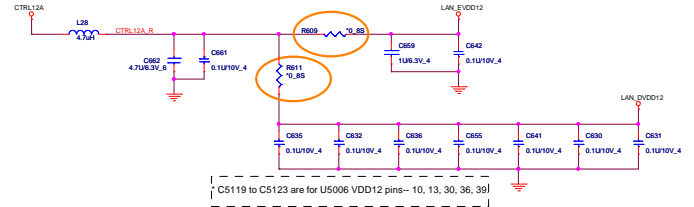
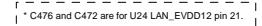
LCDVCC



back light



 PROJECT : LZ2A Quanta Computer Inc.	
Size Custom	Document Number LCD CONN
Date: Thursday, December 01, 2011	Sheet 23 of 43



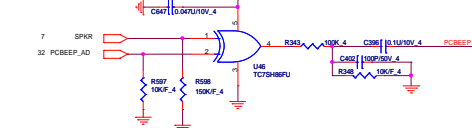
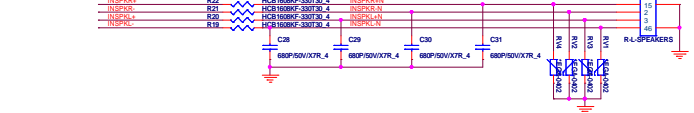
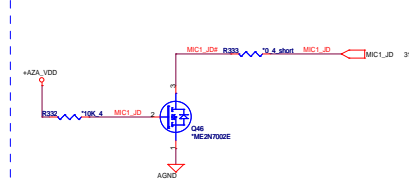
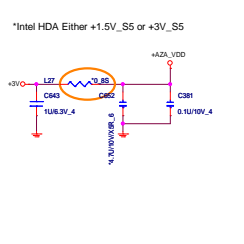
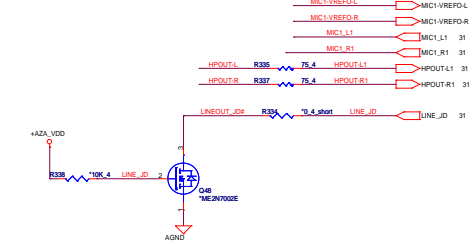
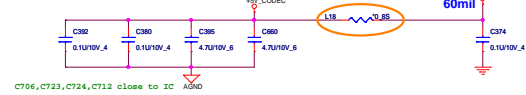
- * C5119 to C5123 are for U5006 VDD12 pins-- 10, 13, 30, 36, 39.

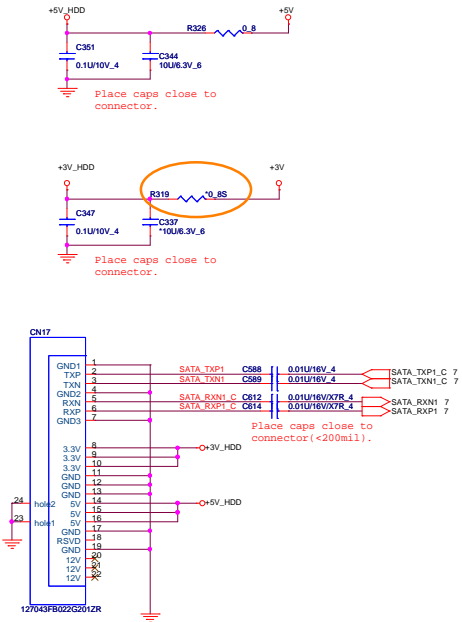
The diagram shows three signals over time:

- Gas Tube Discharge**: A series of pulses labeled D30, D31, D32, and D33. Each pulse is associated with the text "8S201N1LV_1206".
- Reserve for Surge**: A signal that is high during the discharge pulses and low otherwise.
- FOL_EML**: A signal that transitions from high to low at the start of each discharge pulse and remains low.

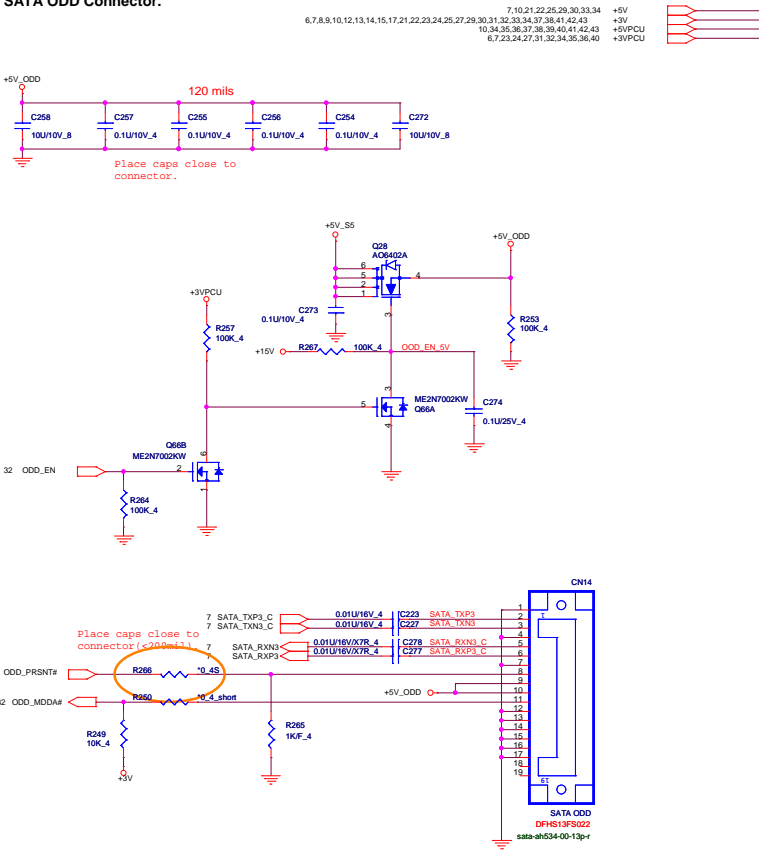
Labels on the left include RS271, D30, D31, D32, and D33. Labels on the right include 75F_8, 0F_8, and FOL_EML.


[illegible]





SATA ODD Connector.

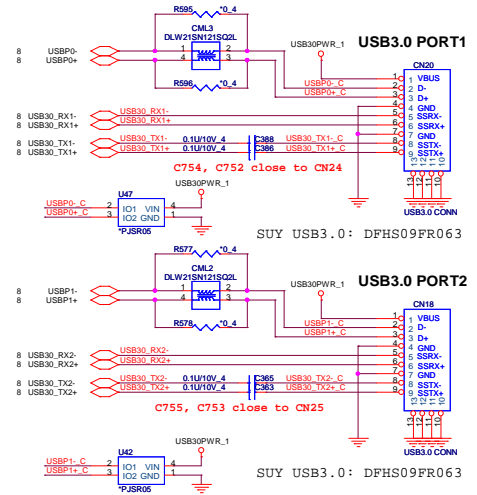
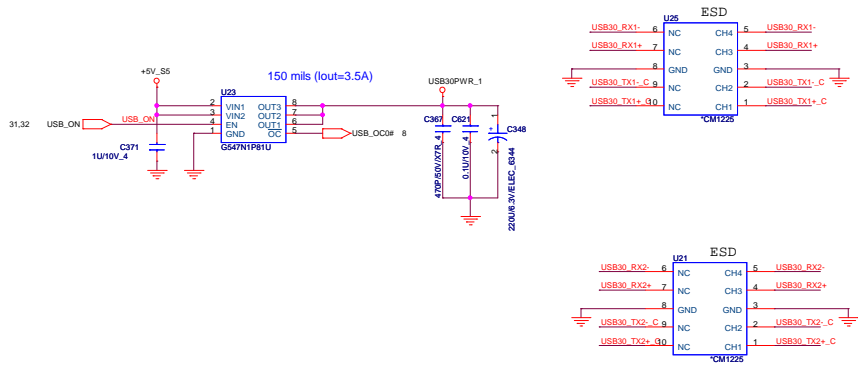




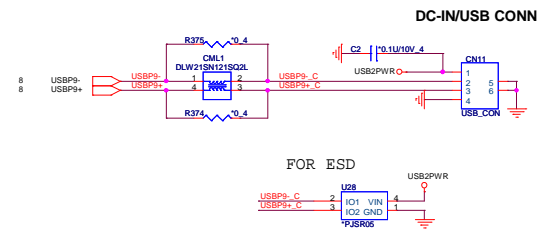
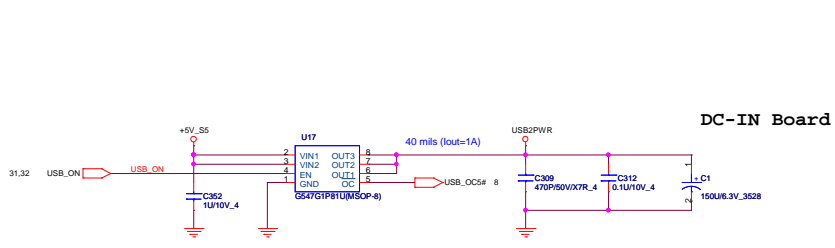
PROJECT : LZ2A
Quanta Computer Inc.

Size	Account Number	Rev
Custom	SATA HDD/CD-ROM	1A
Date:	Thursday, December 01, 2011	Sheet 26 of 43

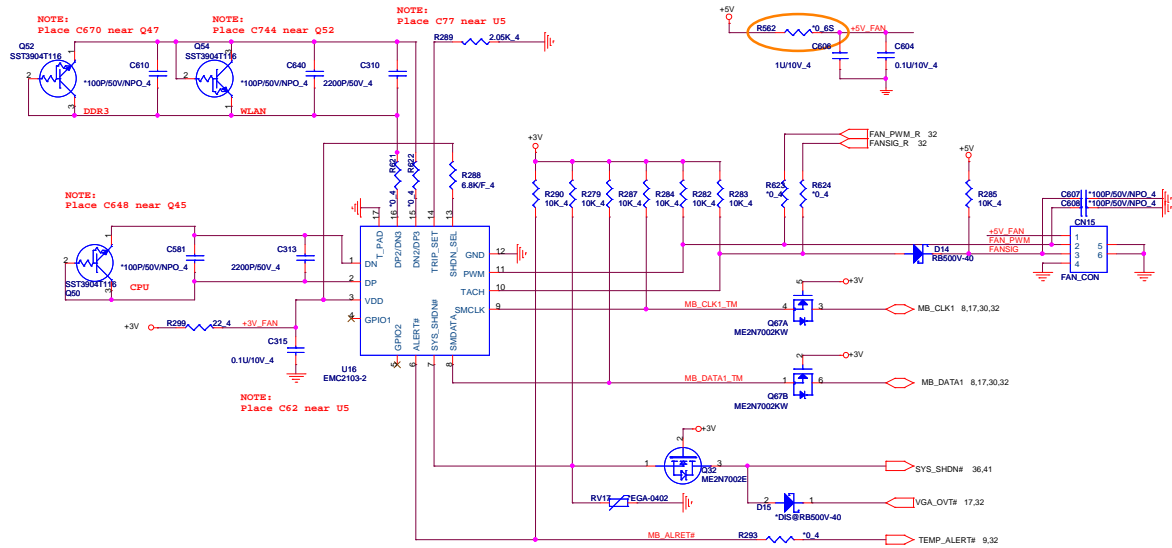
USB3.0*2




USB2.0*1

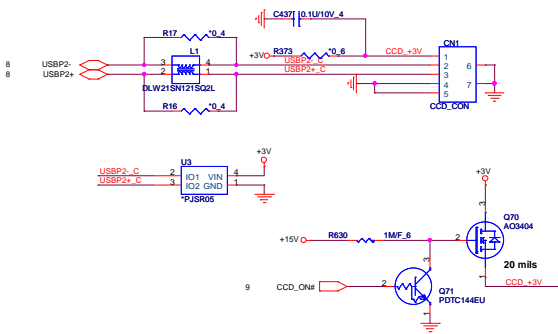


FAN CONTROL

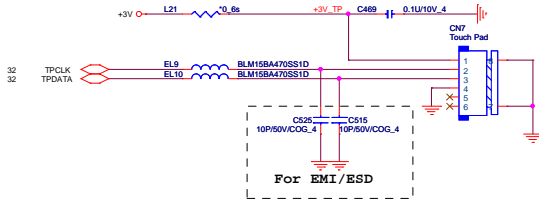


 PROJECT : LZ2A Quanta Computer Inc.		Rev 1A
Size Custom	Document Number FAN /THERMAL	
Date: Thursday, December 01, 2011	Sheet 29 of 43	

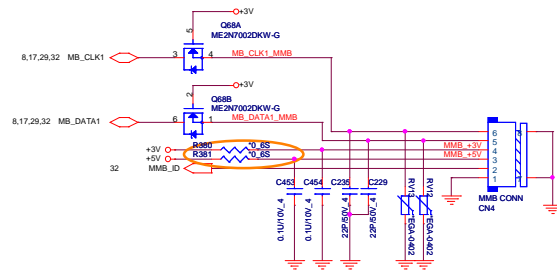
CCD BOARD



Touch pad



MMB

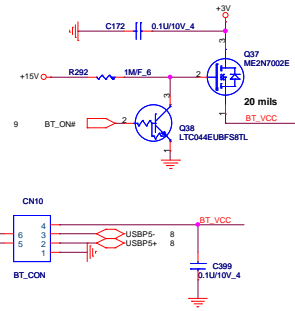


6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,27,29,31,32,33,34,37,38,41,42,43
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23,26,34,36,43



30

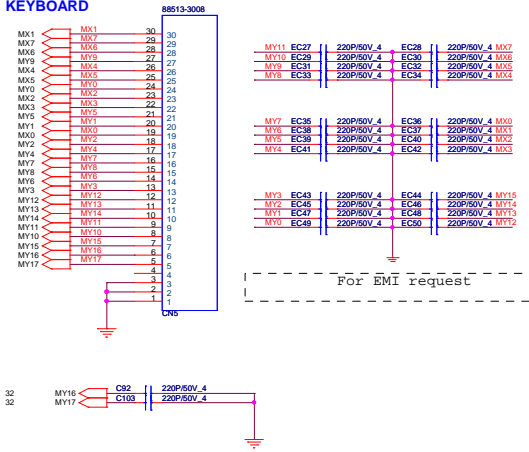
BLUETOOTH



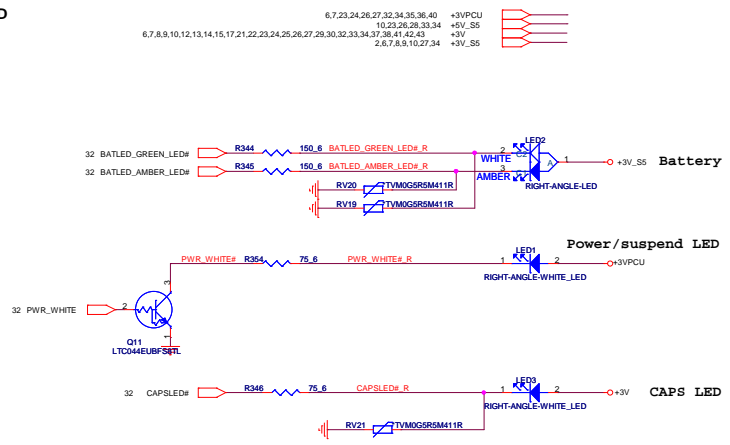
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KEYBOARD

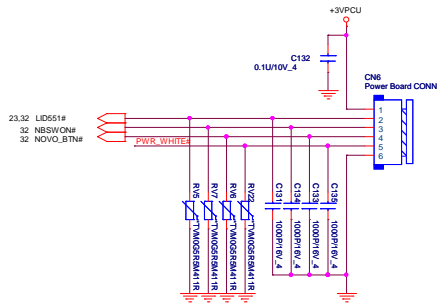


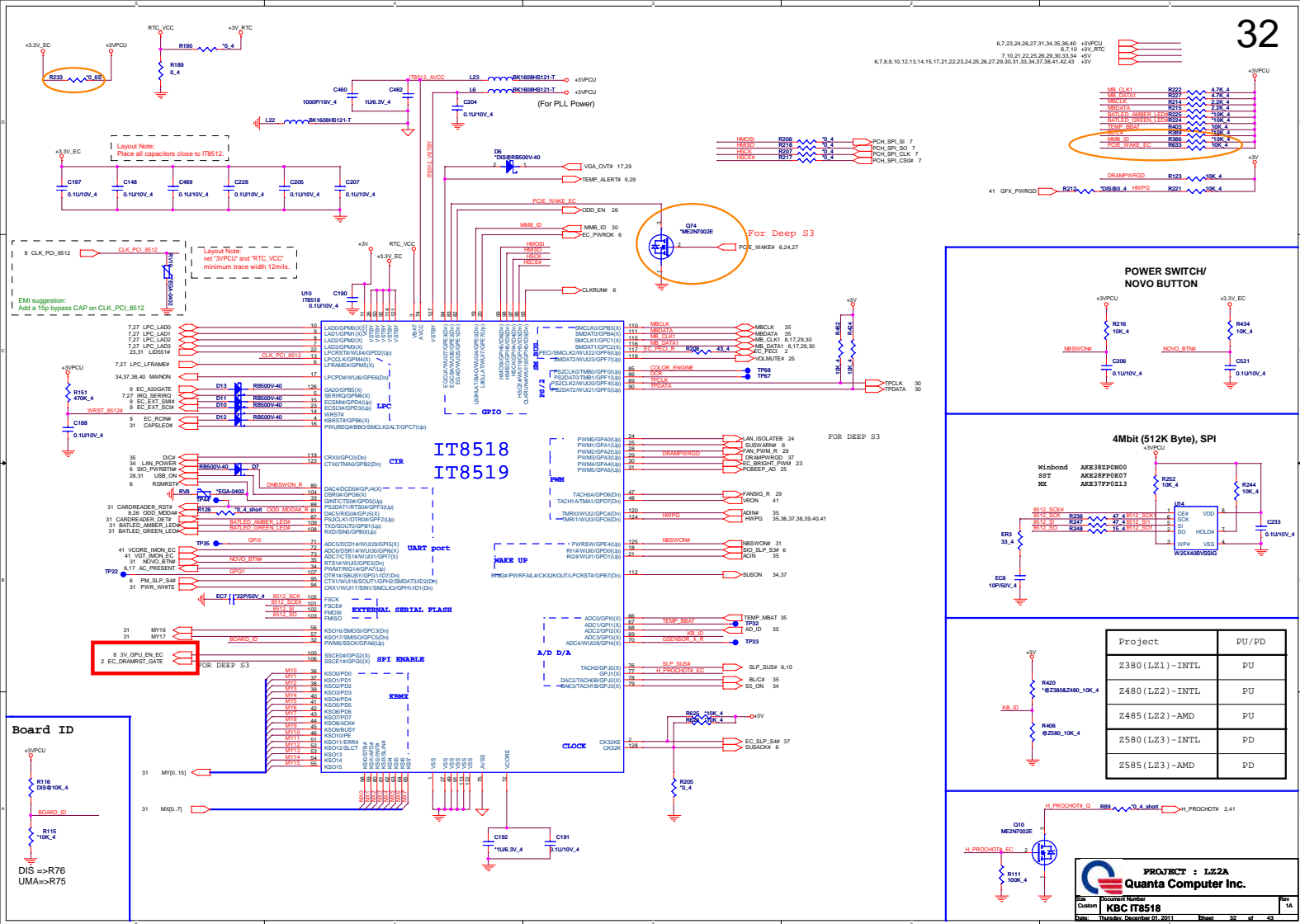
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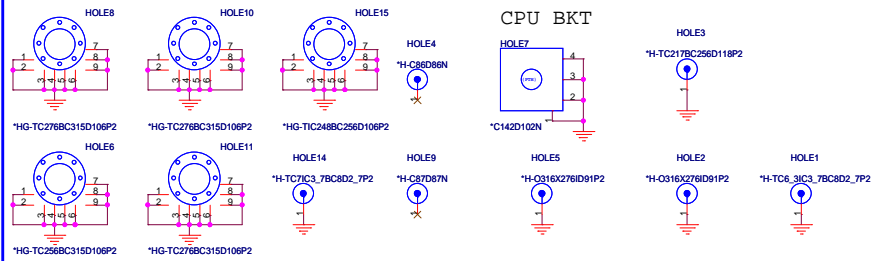


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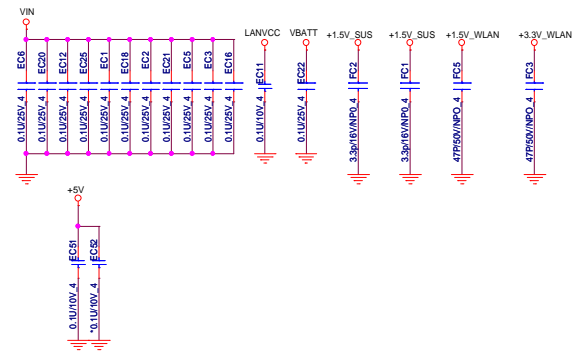
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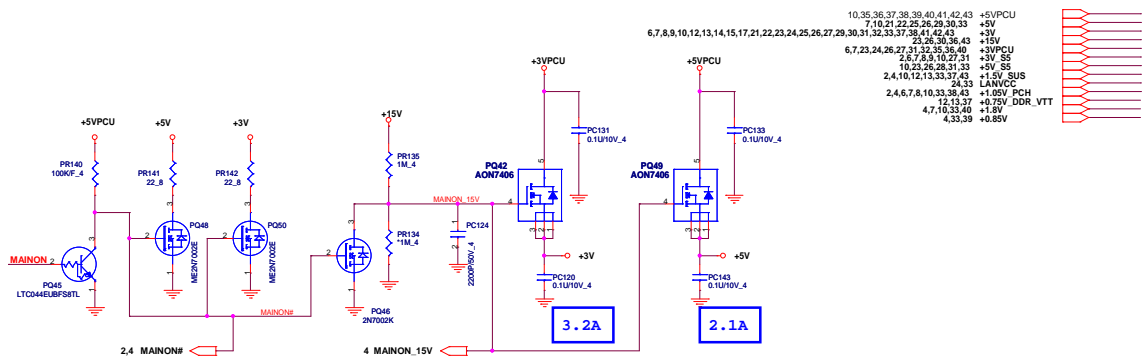




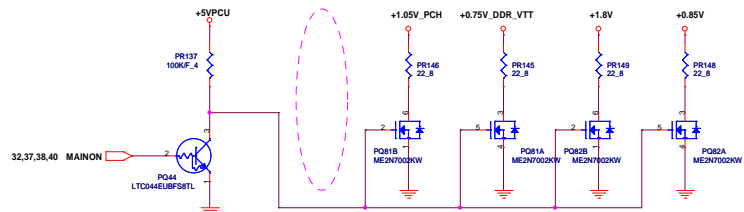
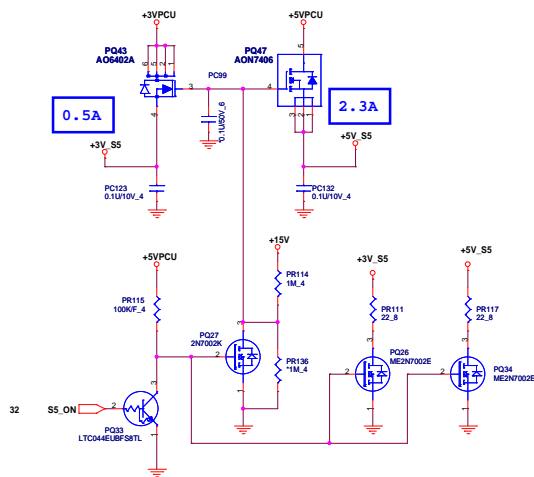


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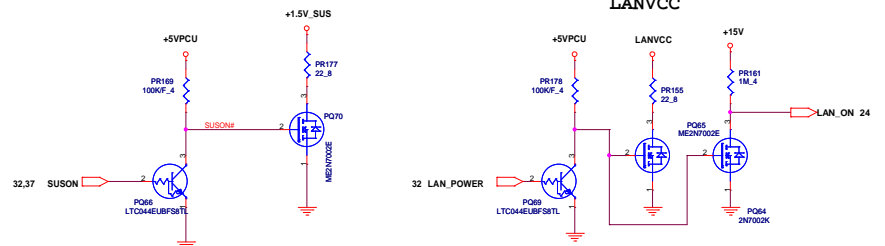


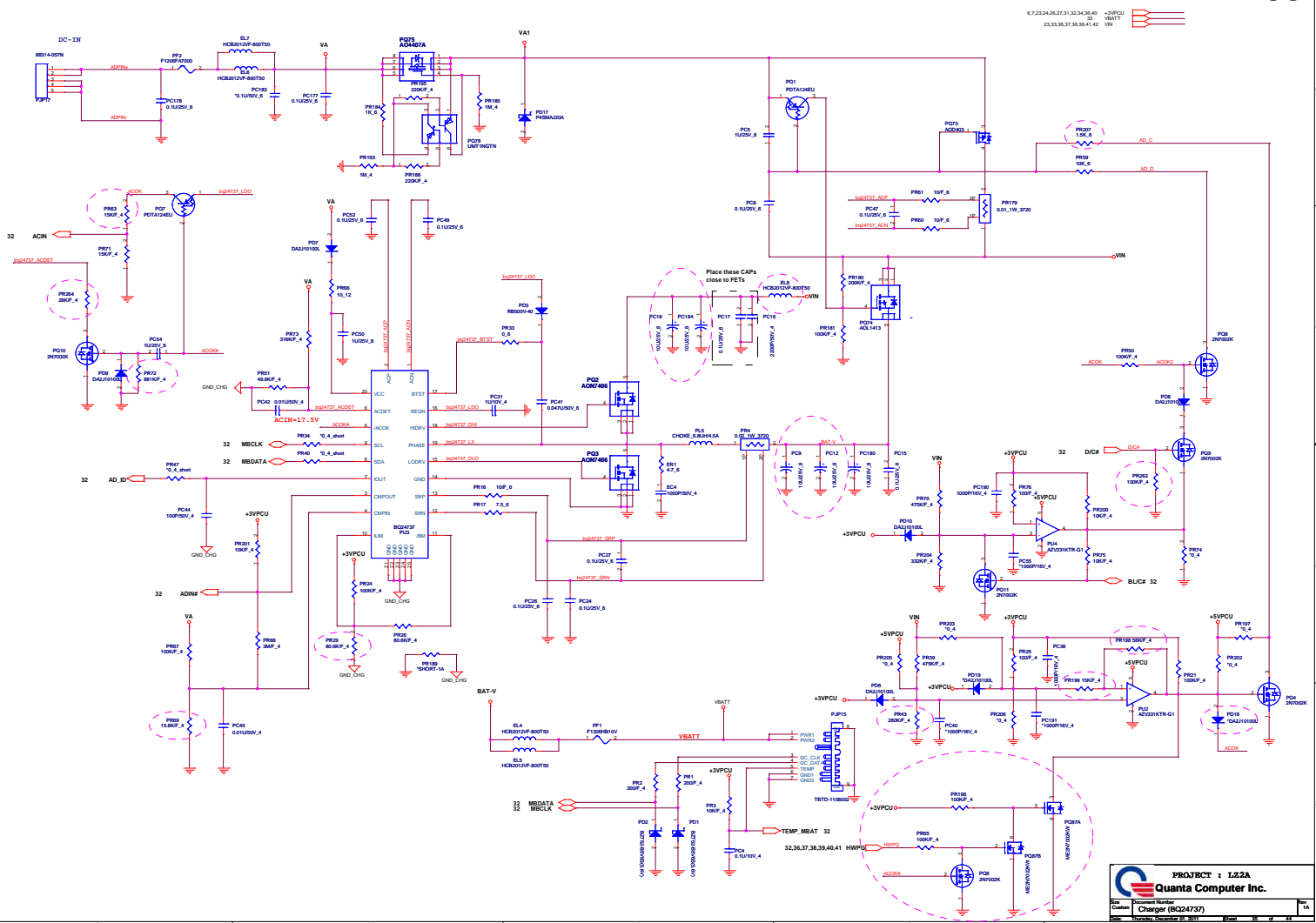


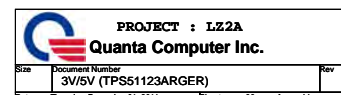
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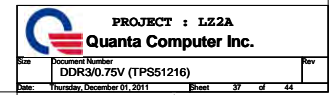


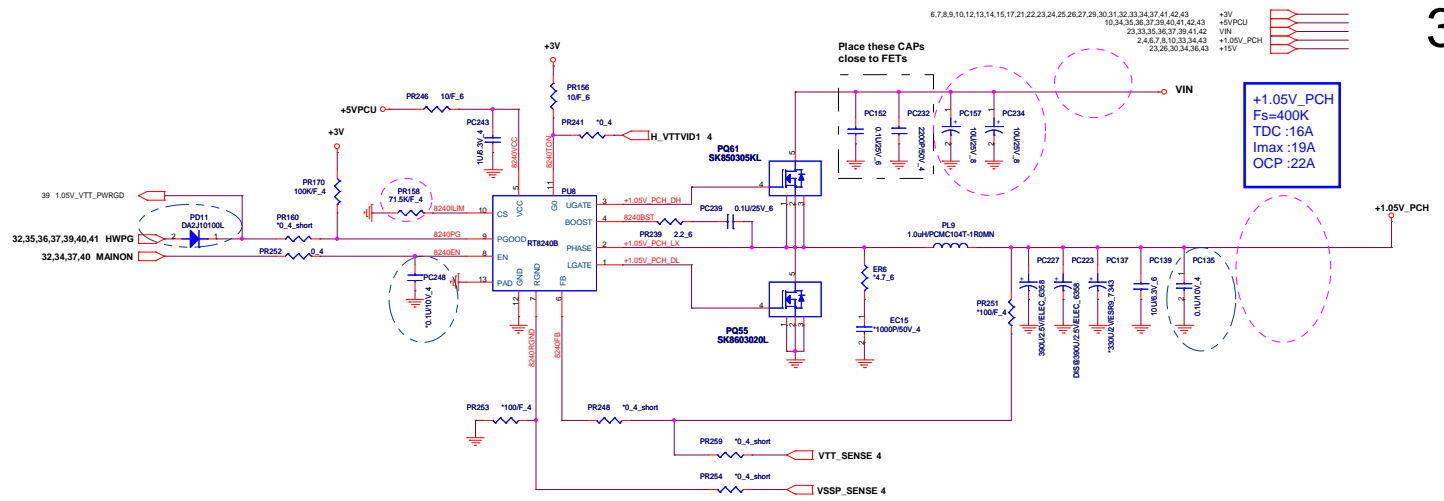
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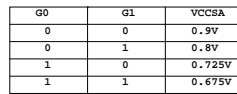


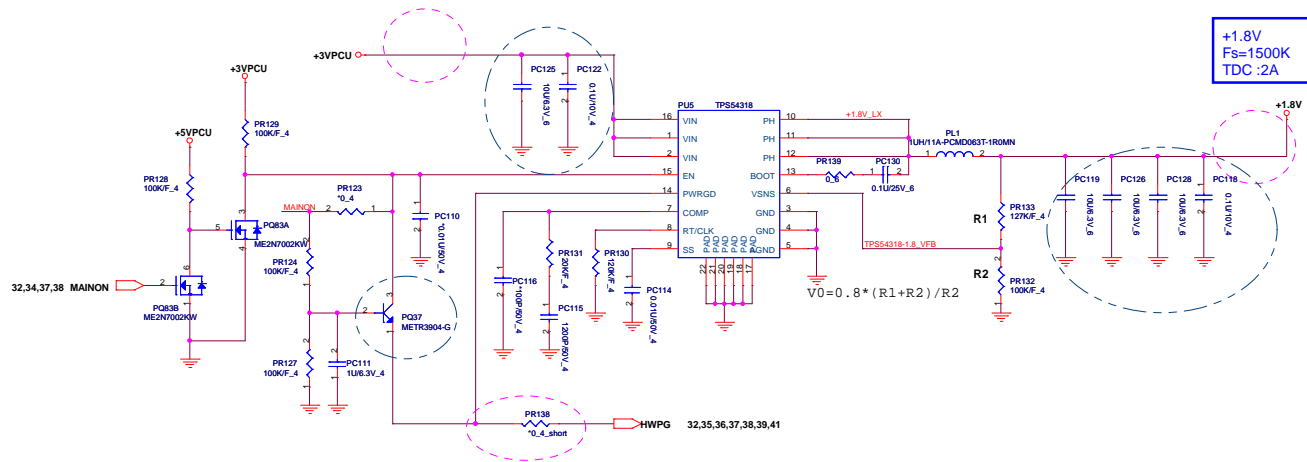







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